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MS-7704

Mini-ITX Ver: 2.3

CPU:
INTEL-Sandy bridge LGA1155

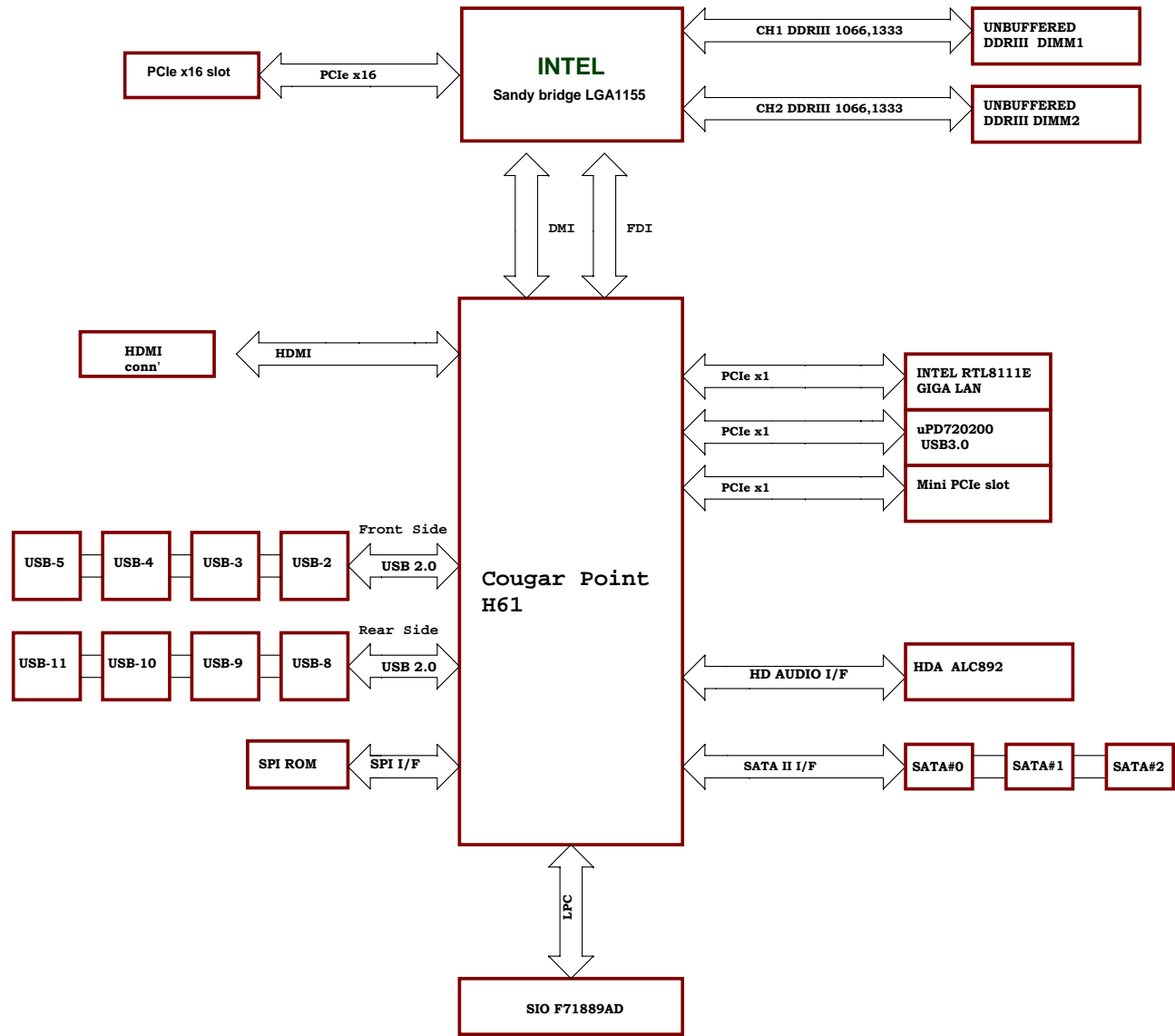
System Chipset:
INTEL-Cougar Point H61

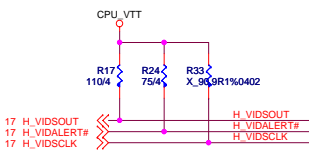
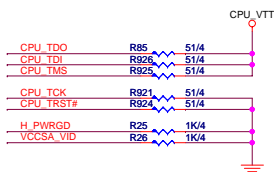
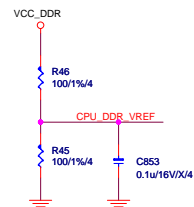
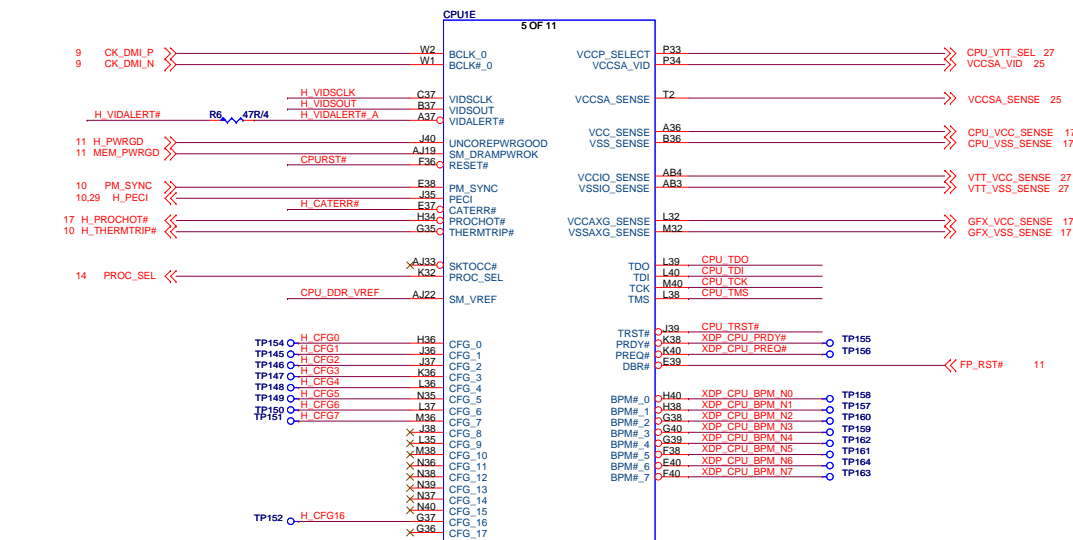
OnBoard Chipset:
HD Audio Codec:ALC892
uPD720202 USB3.0
LAN-RTL8111E
SIO:Fintek F71889AD
Flash ROM: 64 Mb SPI

Main Memory:
DDRIII (1066/1333MHz) * 2 (Dual Channel)

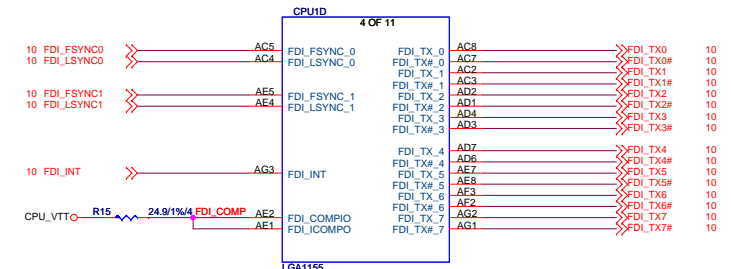
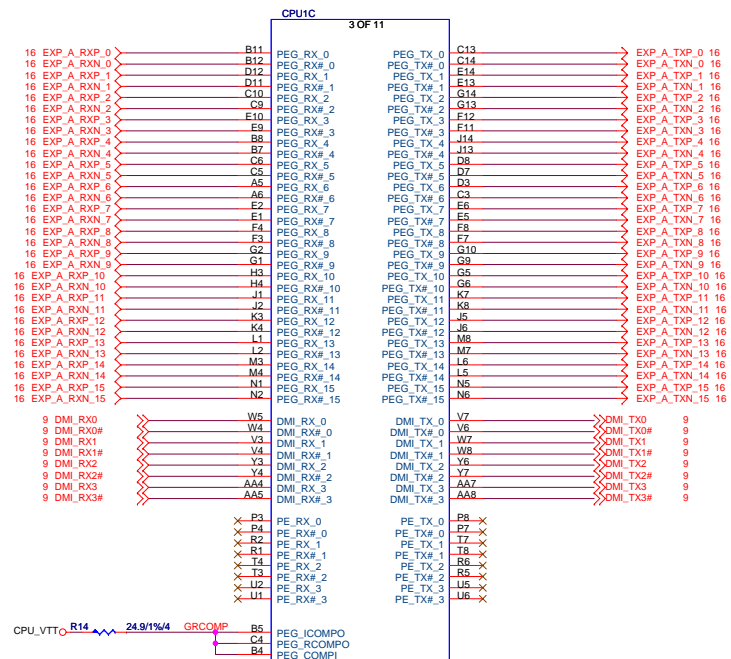
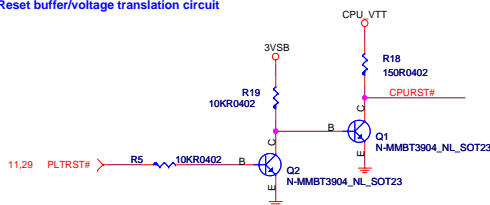
Expansion Slots:
PCI Express (X16) Slot * 1
Mini PCIe(X1) Slot * 1

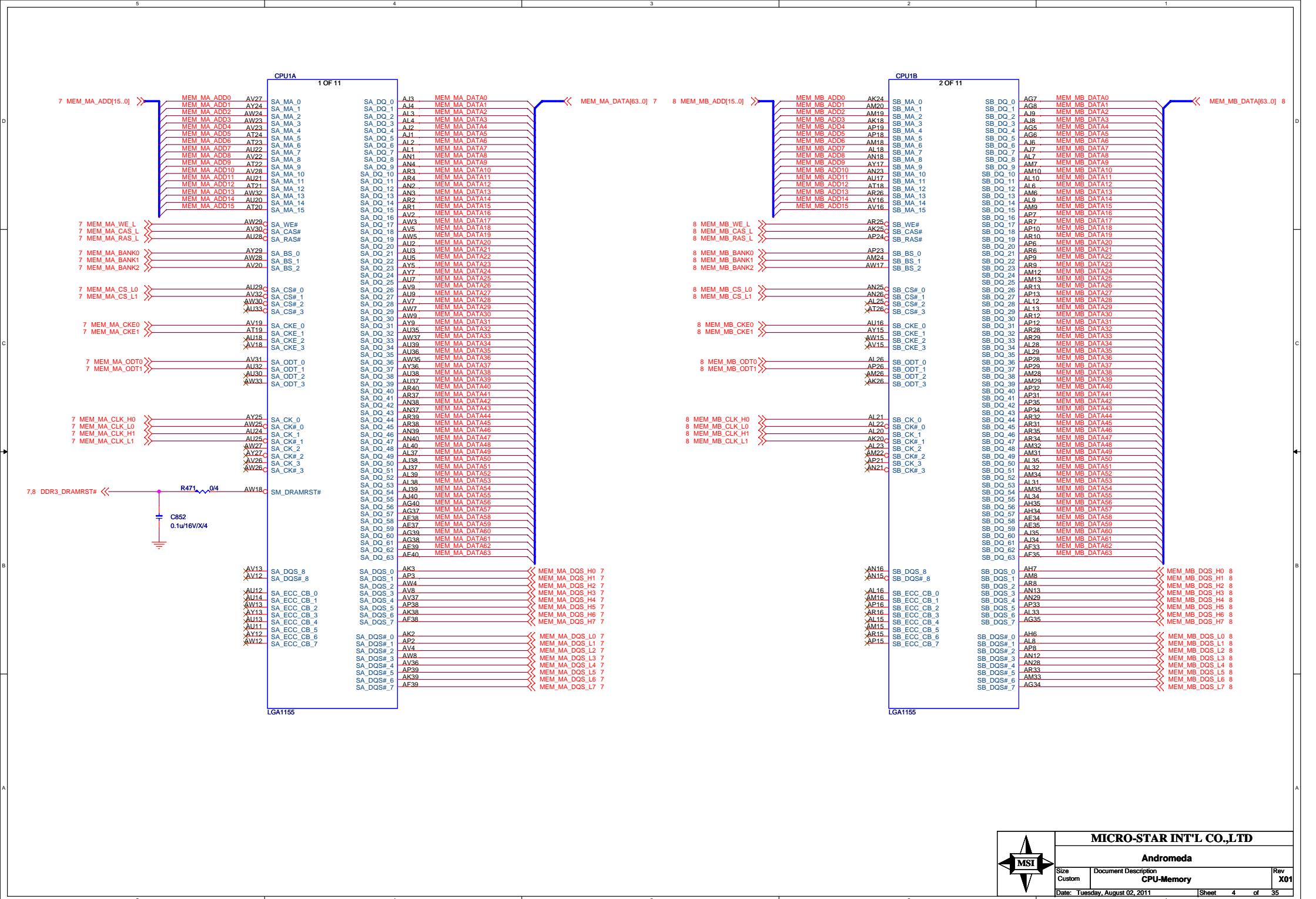
PWM:
VRD12 ISL6364 4+1 Phase Dr.MOS

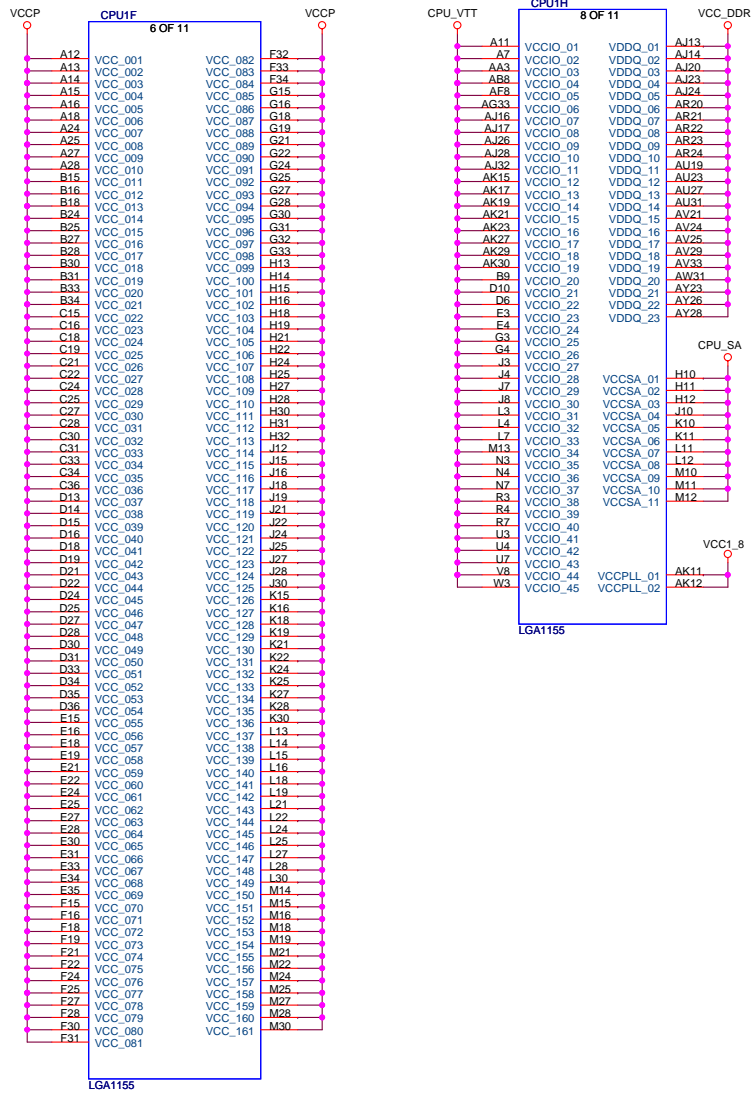




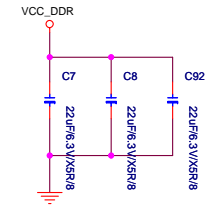
Reset buffer/voltage translation circuit





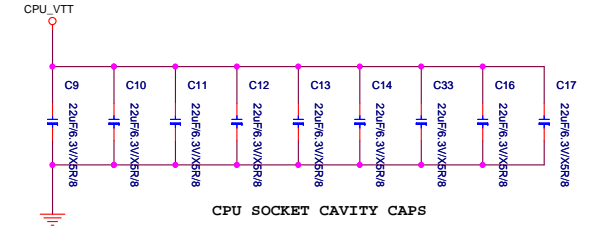


+1.5V_DDR3-Decoupling

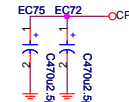


CPU SOCKET CAVITY CAPS

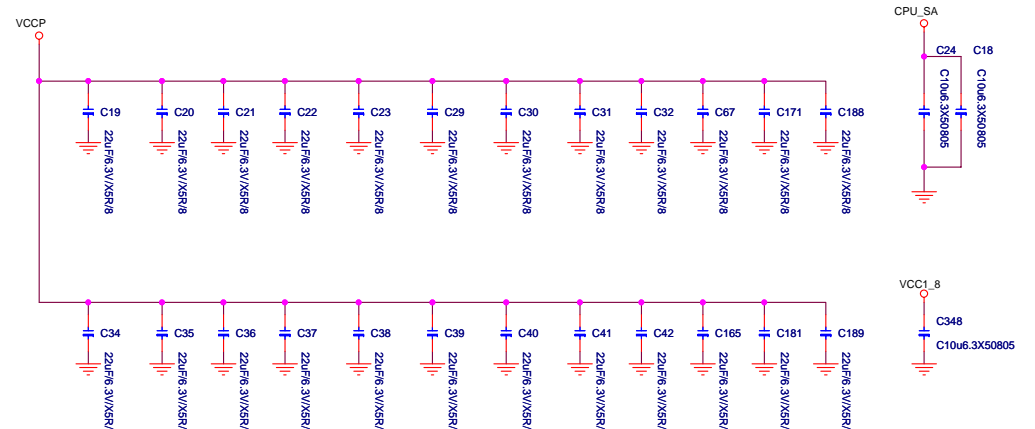
+CPU_VTT Decoupling



bottom SP Capacitors



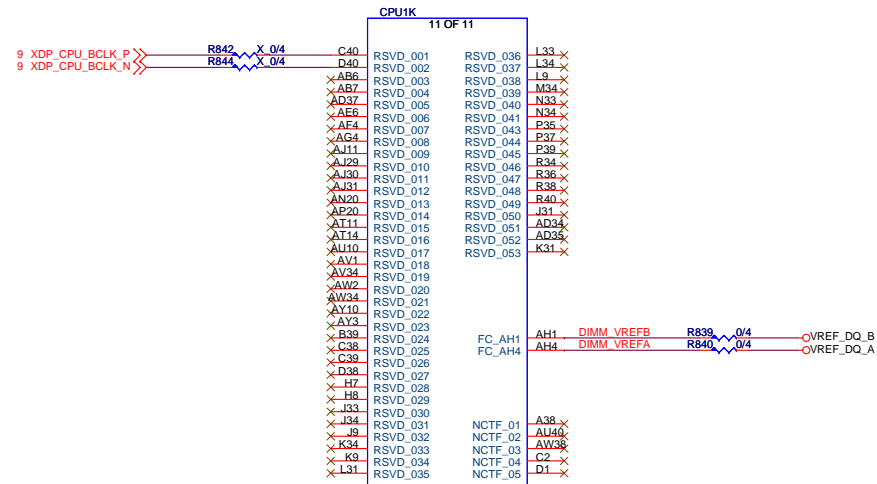
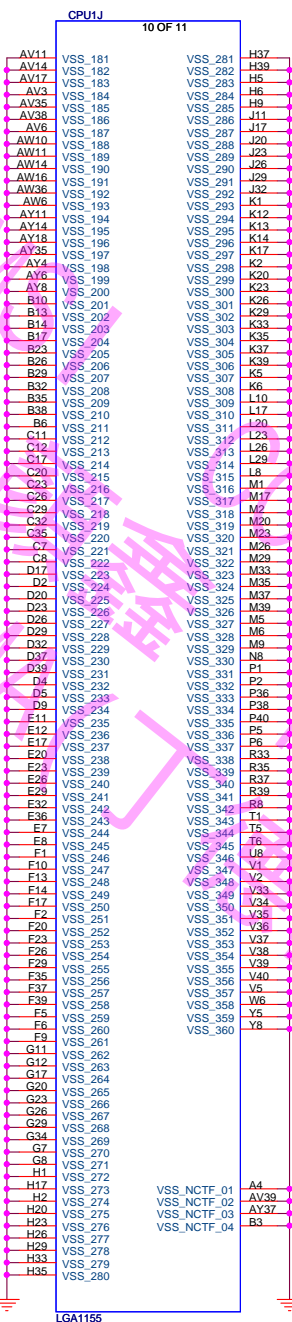
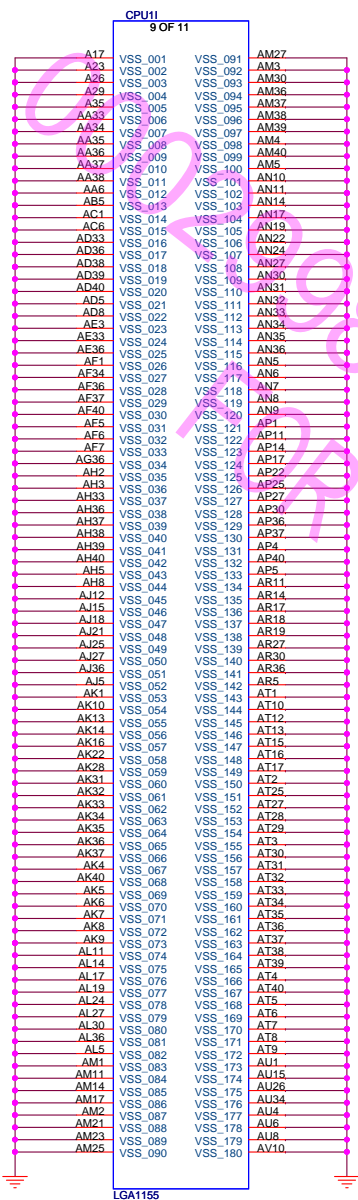
+CPU_VCCP-Decoupling



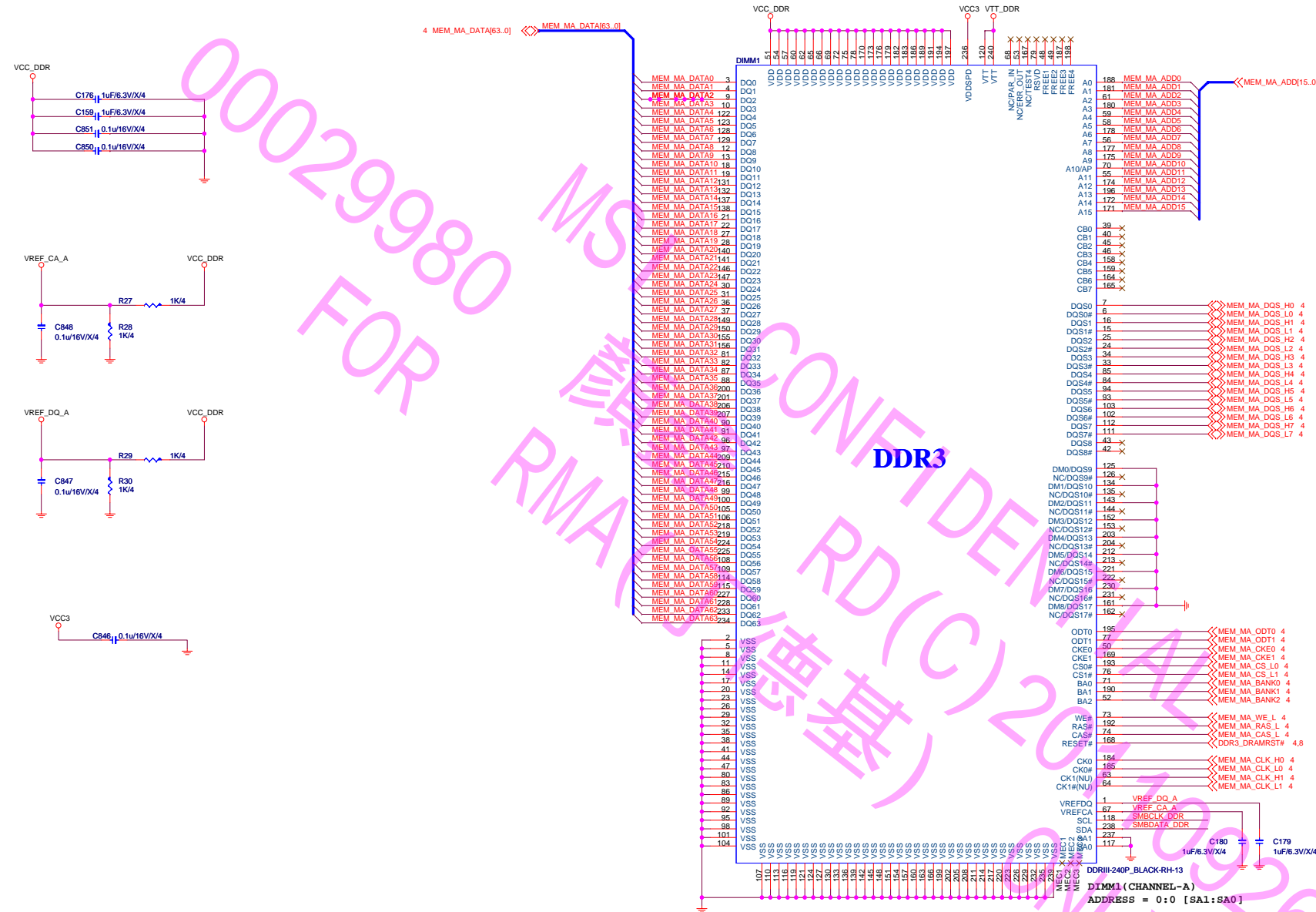
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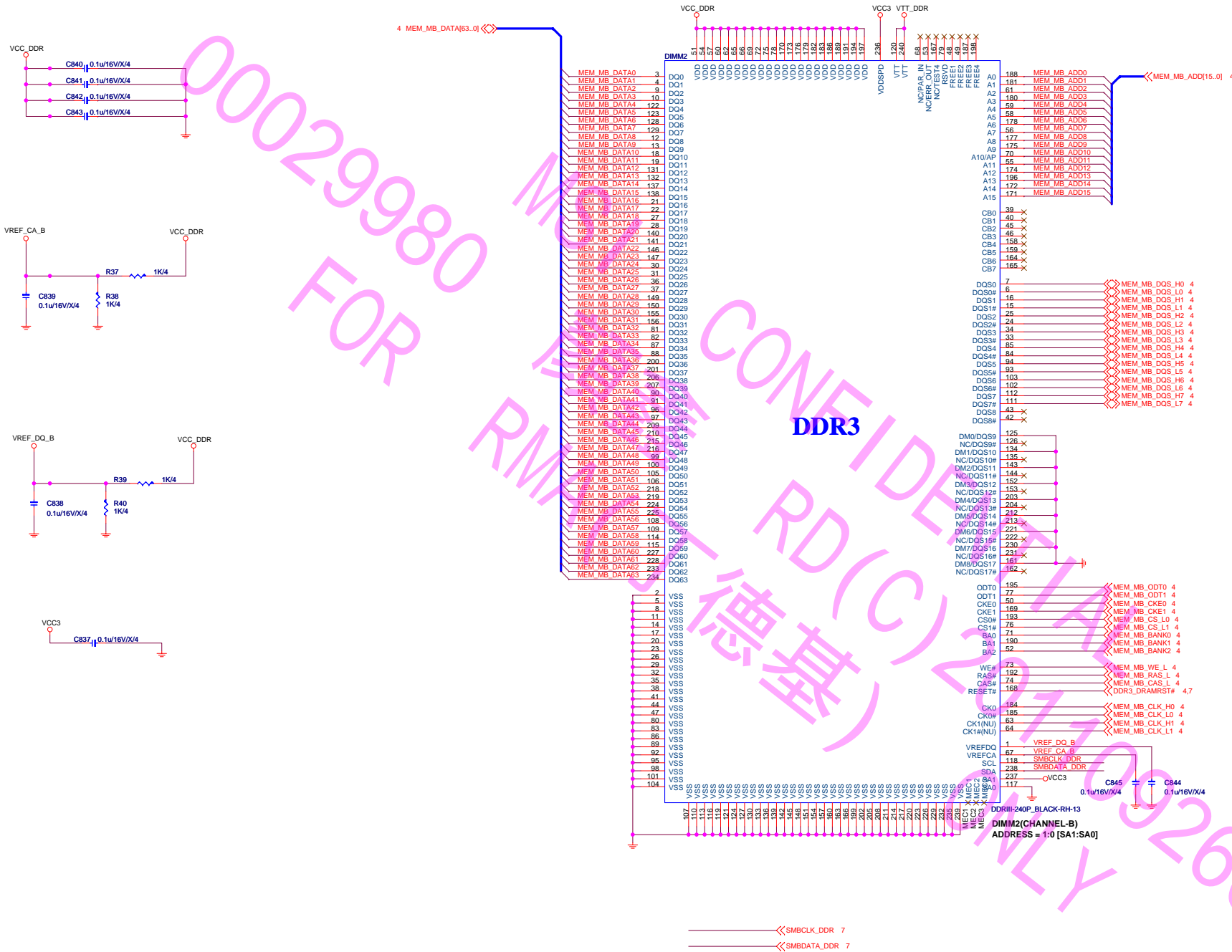


DDR3 DIMM1_A0



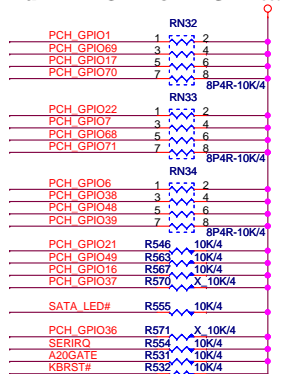
8 SMBCLK_DDR >> R34 33R/4 >> SMBCLK 11,16,28,30
8 SMBDATA_DDR >> R36 33R/4 >> SMBDATA 11,16,28,30

DDR3 DIMM2_B0

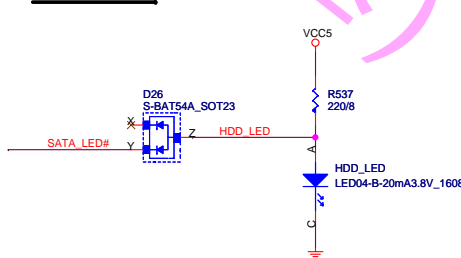


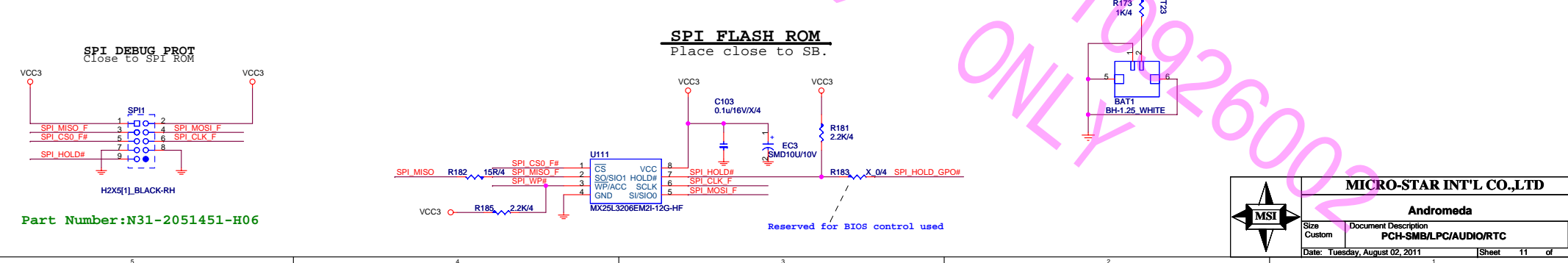
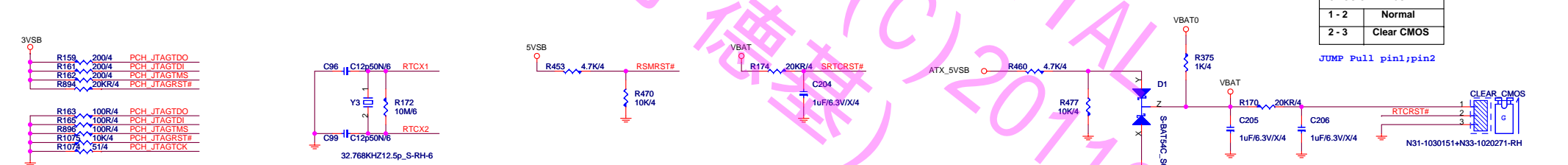
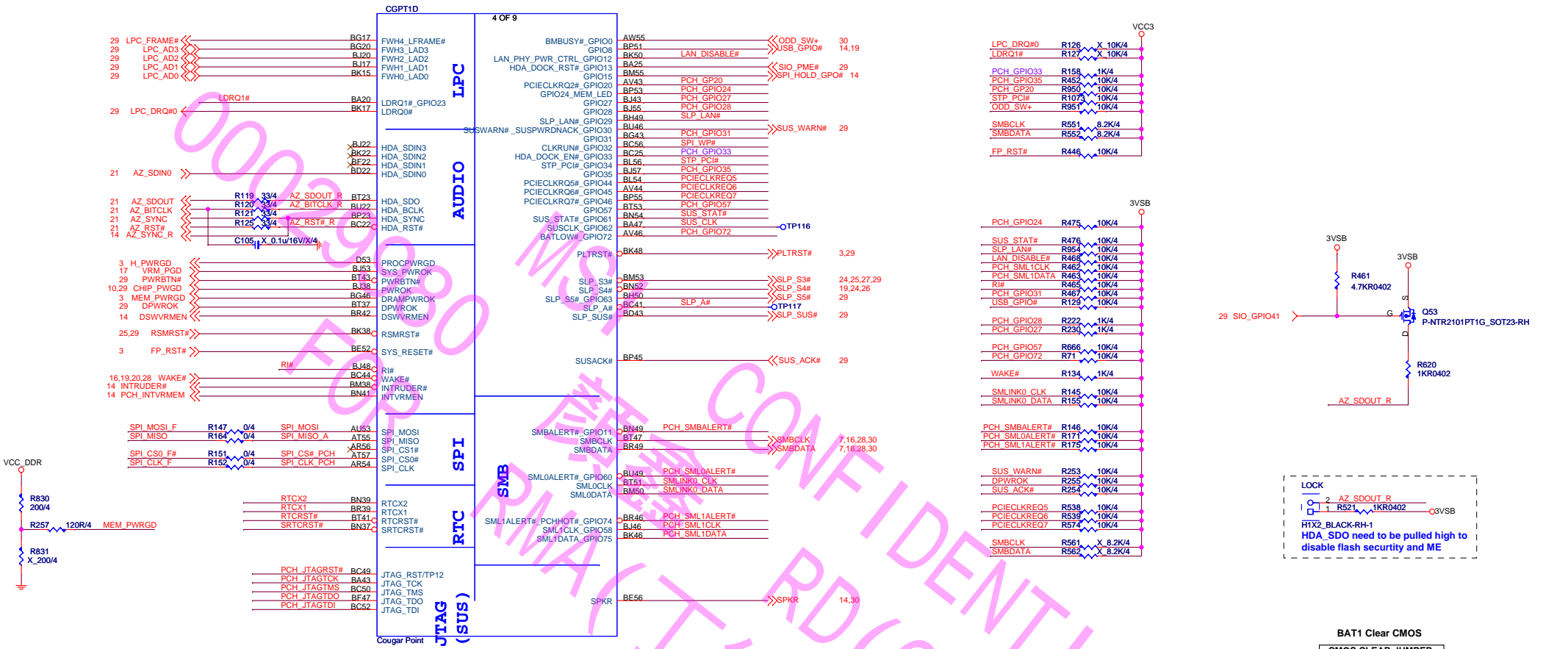


Pull HIGH for PCH



HDD LED





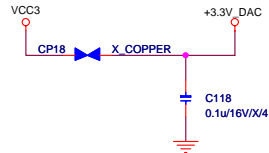
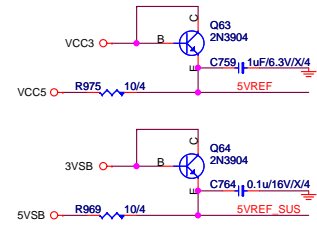
BAT1 Clear CMOS

CMOS CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear CMOS

JUMP Pull pin1;pin2

LOCK
1 2 AZ_SDOUT R
R521 1KR0402 3VSB
H1X2_BLACK-RH-1
HDA_SDO need to be pulled high to
disable flash security and ME

SPI FLASH ROM
Place close to SB.



PCH_1P05

R194 X 0/8

VCCAPLLDMI2

C195 X_10uF/6.3V/X5R/8

C146 X_1uF/6.3V/X5R/4

R196 0/8

VCCCLLDMI

C197 C10u6.3X50R5-H-3

C196 1uF/6.3V/X/4

R187 0/8

VCCA_DPLL A

C108 1uF/6.3V/X/4

R188 0/8

VCCA_DPLL B

C109 1uF/6.3V/X/4

PCH_1P05

L28

VCCAPLLEXP

X_L1U_500mA_0805

C114 X_10uF/6.3V/X5R/8

C198 X_1uF/6.3V/X5R/4

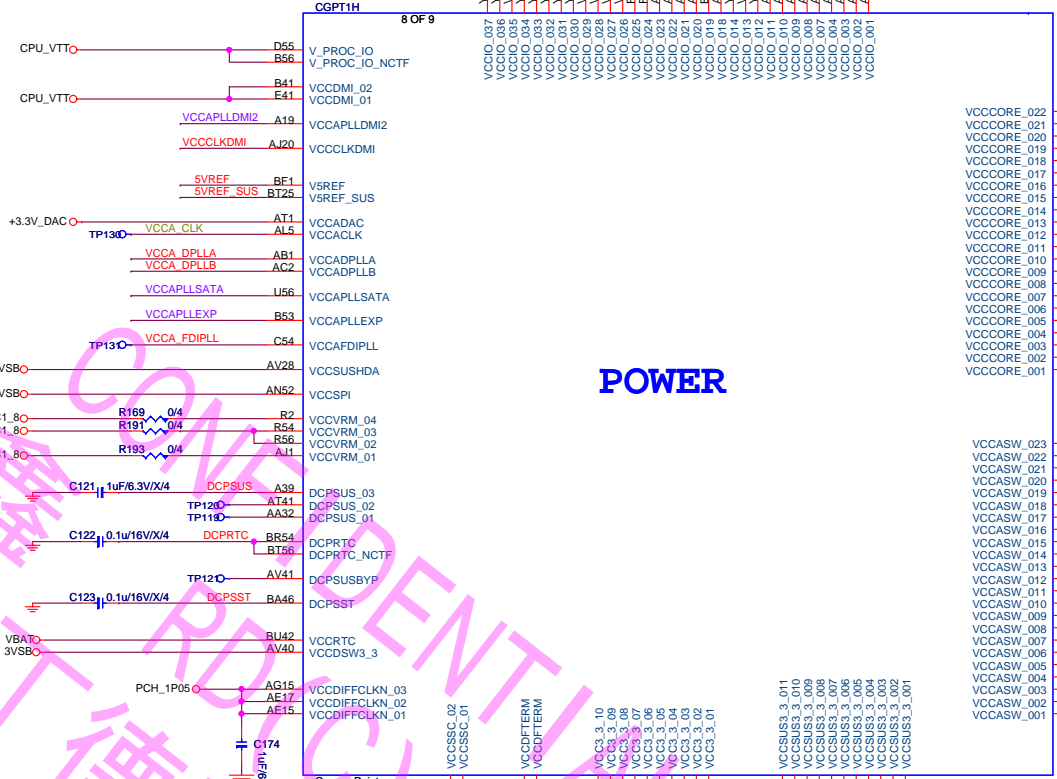
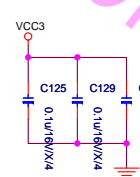
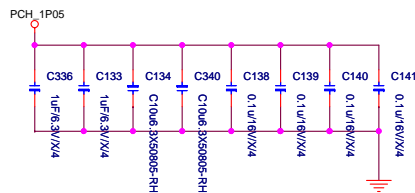
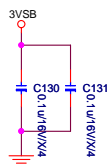
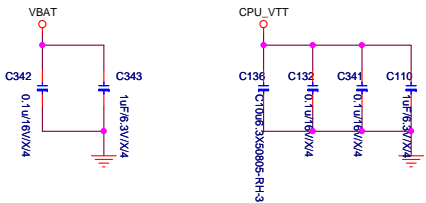
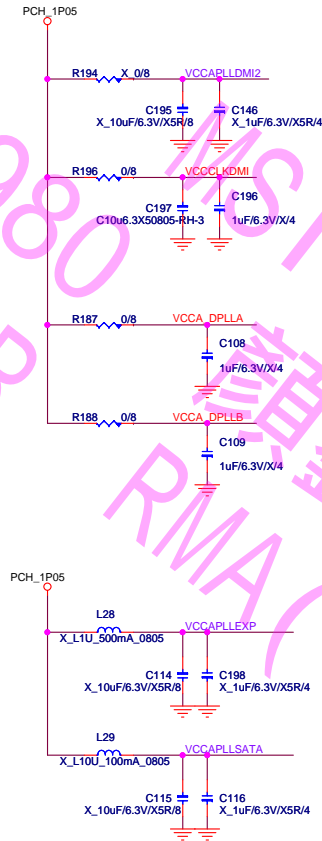
L29

VCCAPLLSATA

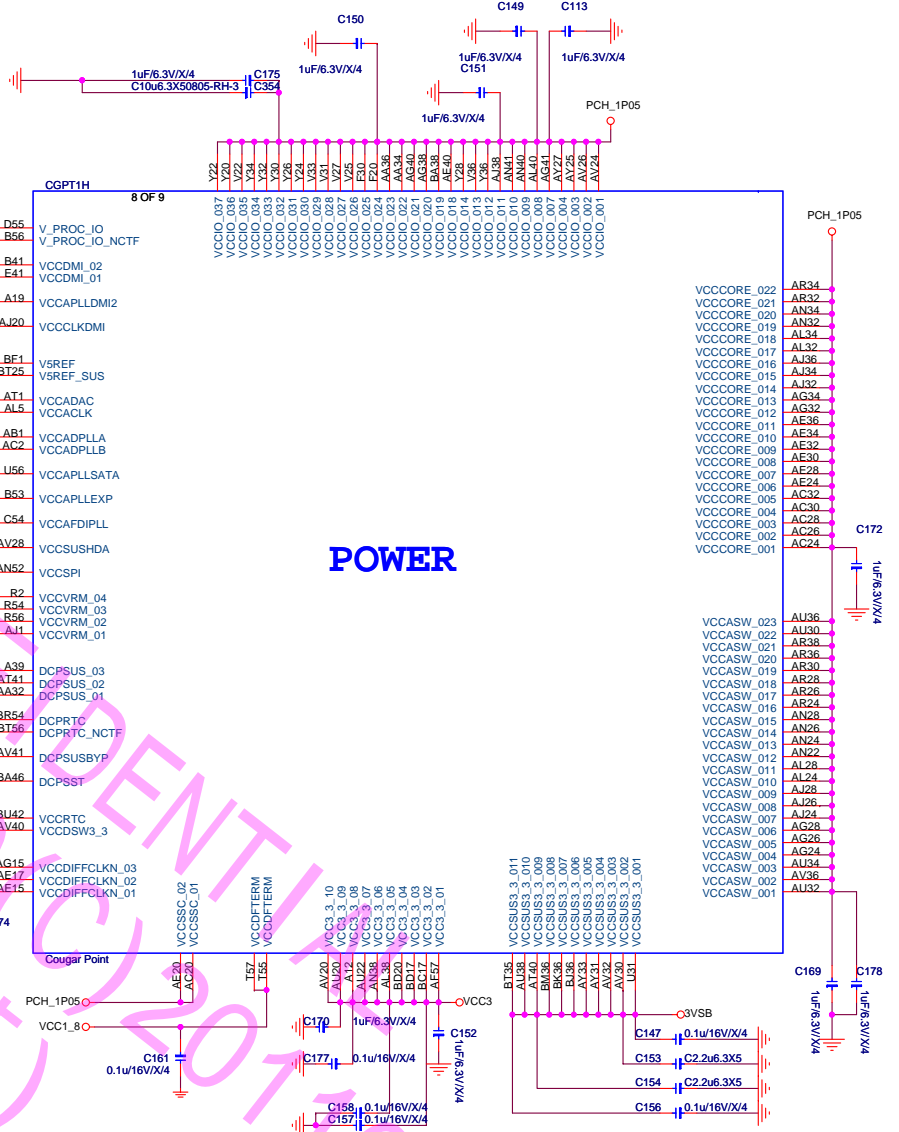
X_L1U_100mA_0805

C115 X_10uF/6.3V/X5R/8

C116 X_1uF/6.3V/X5R/4

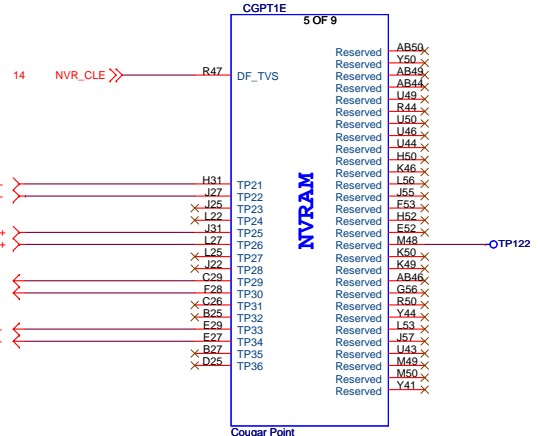


POWER



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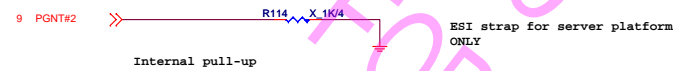
Size Custom	Document Description PCH -POWER	Rev X01
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BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	0
SPI	1	1



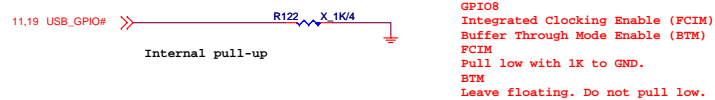
WEAK INTERNAL PULLUPS ON GNT1#



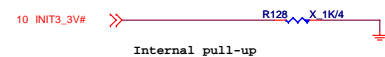
Internal pull-up



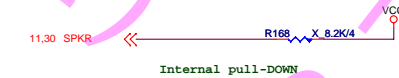
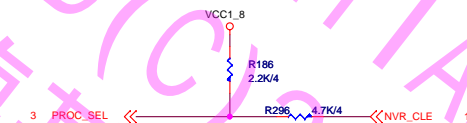
Internal pull-up



Internal pull-up



Internal pull-up



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0: Disable Internal Deep Sleep 1.05 V regulators.
1: Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

HDA_SYNC
On die PLL VR volatge selector

GPIO15
Default (Disable TLS):
Leave NC. Internal pull down.

DMI/FDI TERMINATION VOLTAGE
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

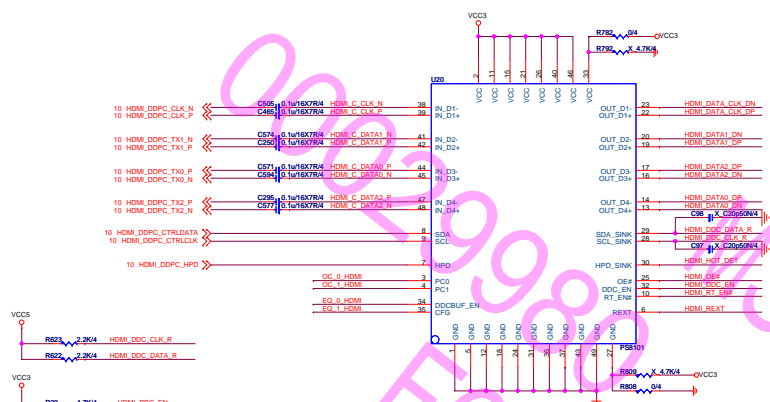
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



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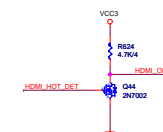
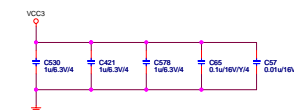
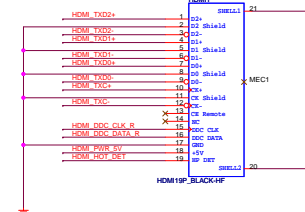
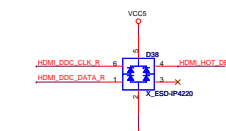
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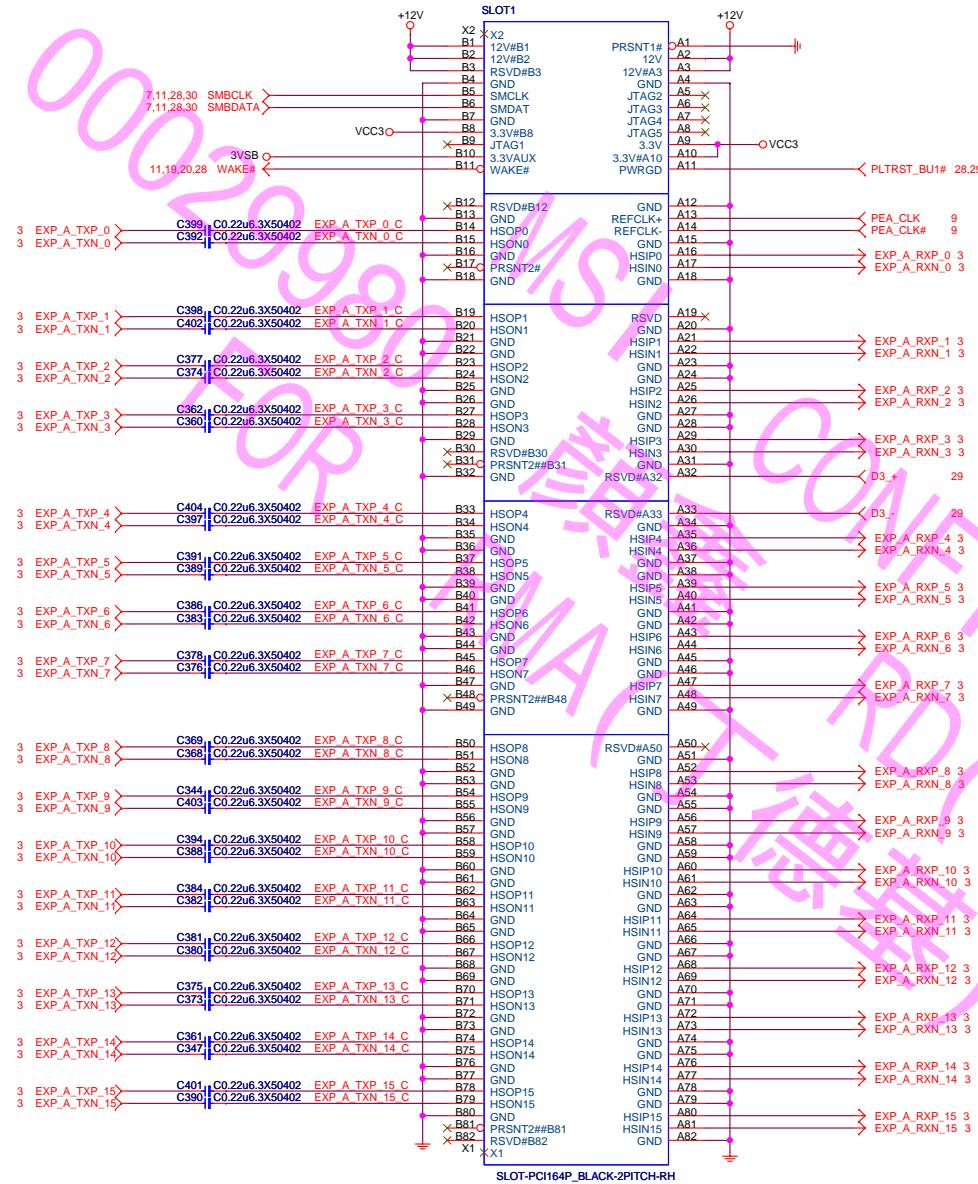
PARADE PN:B0B-081010C-P97

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	input 50 ohm termination resistor enable	the input termination resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCRUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

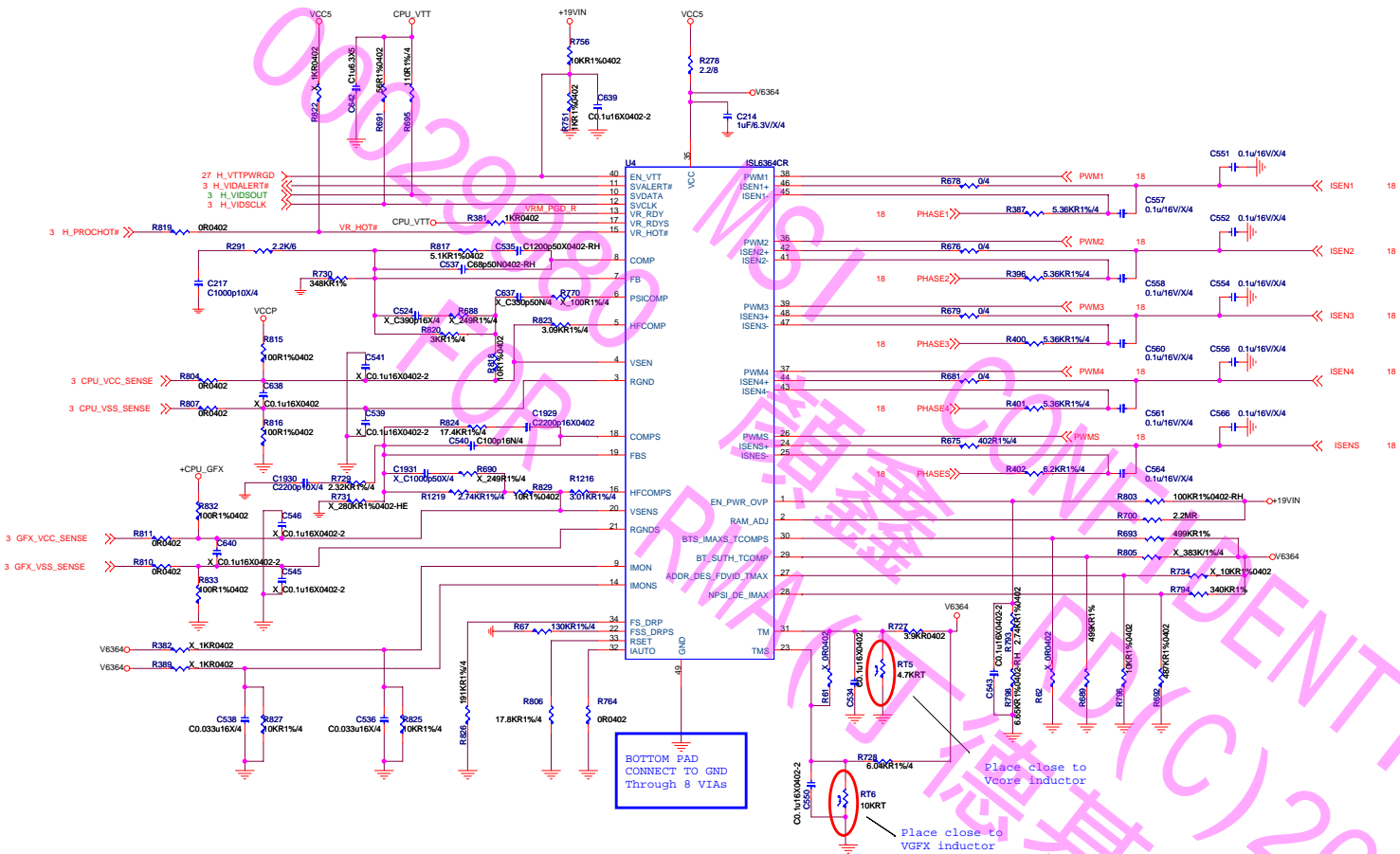
DDC_EN, DDCRUF_EN, OE#	DDC Passive Switch	DDC Active Buffer	PCI, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB



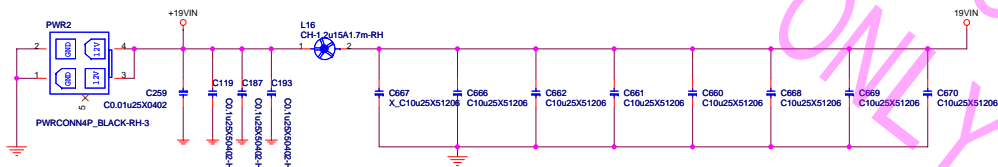
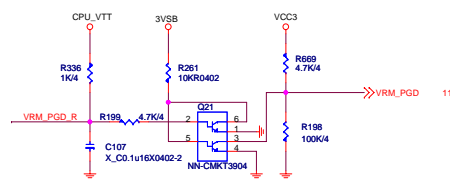
PCI EXPRESS X16 SLOT

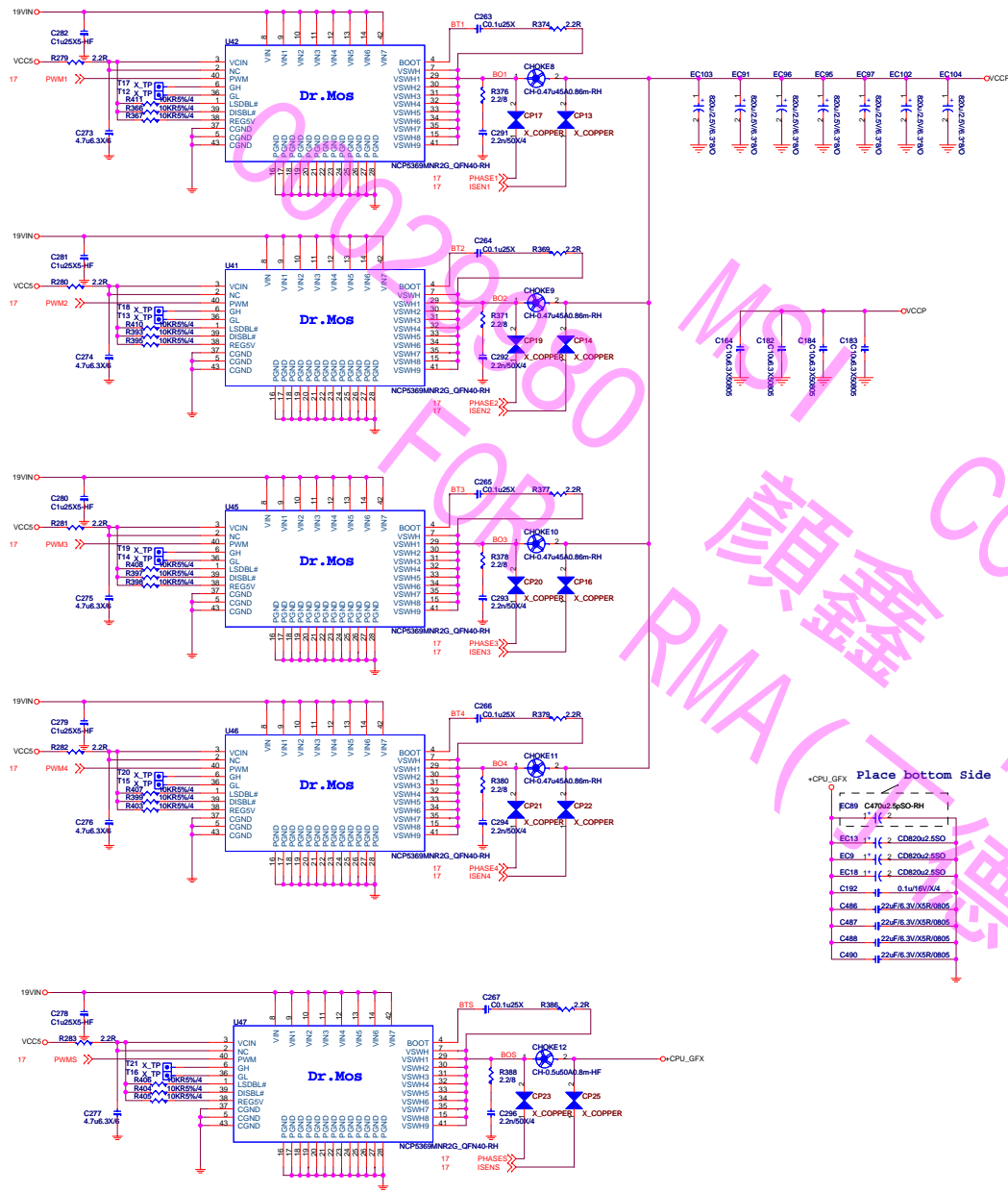


VOLTAGE REGULATOR MODULE (VRD12)



VRMPWRGD LEVEL SHIFT





+CPU_GFX Place bottom Side

EC89	C4702	5S0-RH
EC13	1	2 C08202 5S0
EC9	1	2 C08202 5S0
EC18	1	2 C08202 5S0
C192	1	0.1u16V/0V4
C486	1	22uF/6.3V/X5R/0805
C487	1	22uF/6.3V/X5R/0805
C488	1	22uF/6.3V/X5R/0805
C490	1	22uF/6.3V/X5R/0805



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Site Custom

Document Description

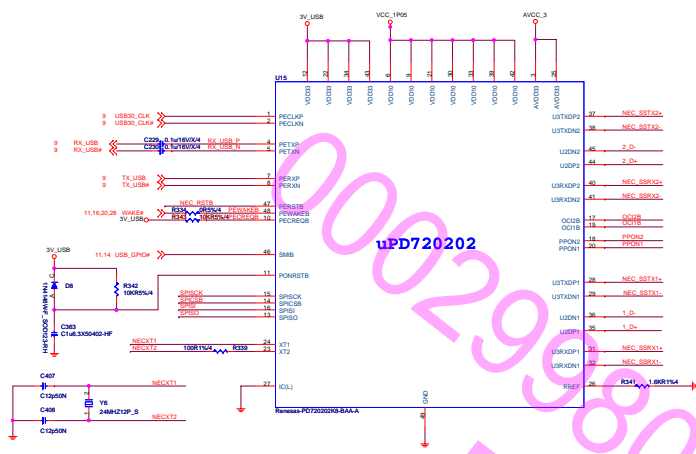
Dr.MOS

Date: Tuesday, August 02, 2011

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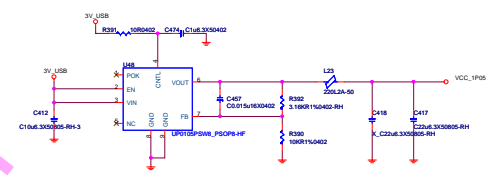
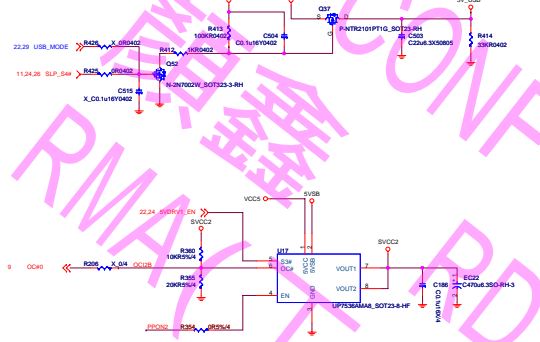
Rev

X01

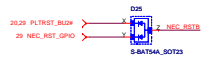
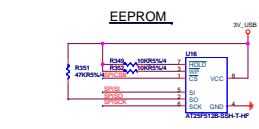
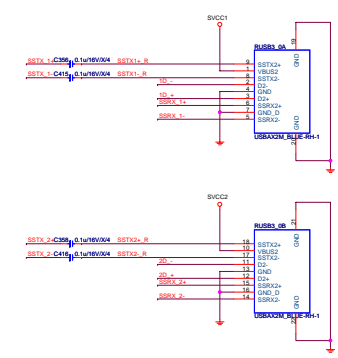


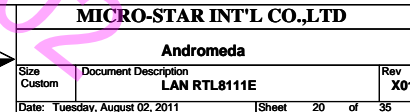
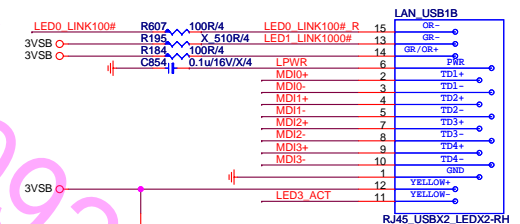
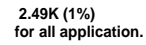
uPD720202

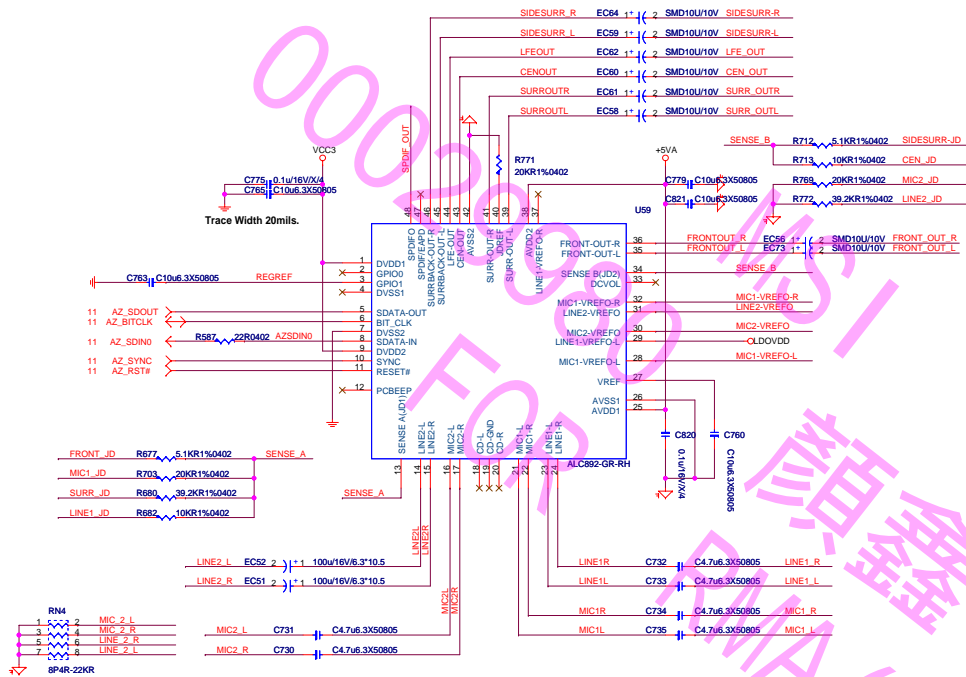
3V Dual Circuit



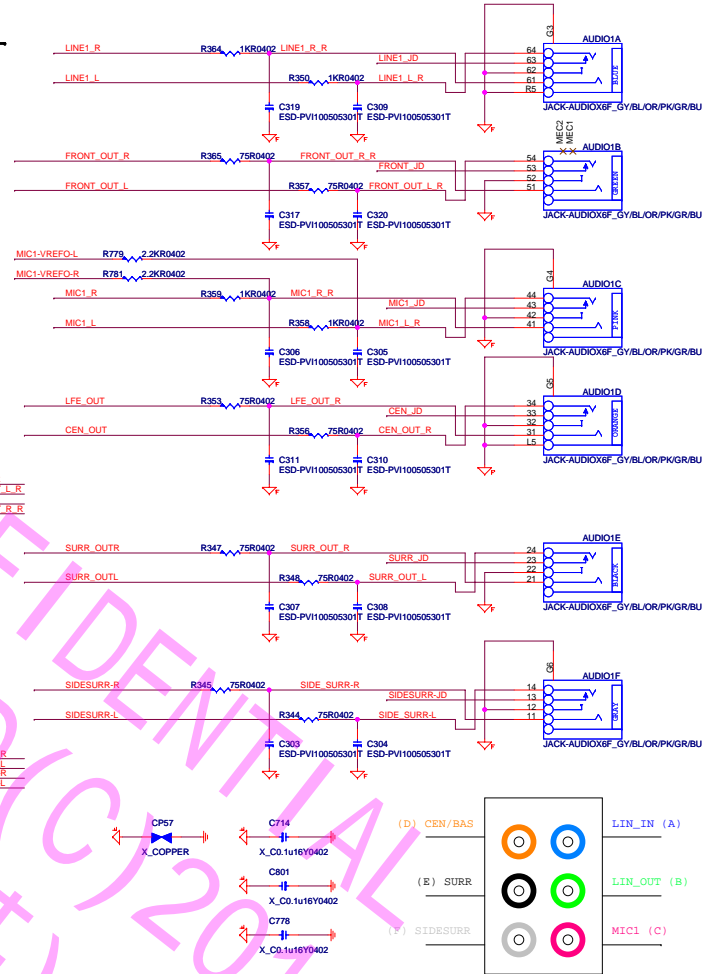
REAR USB3.0 Connector



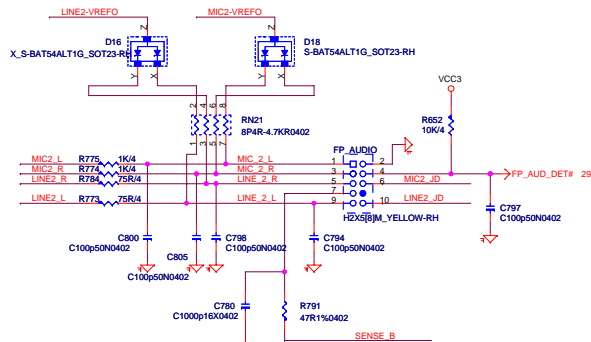




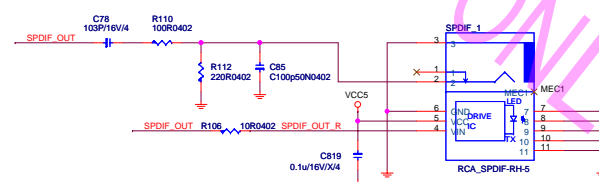
Rear audio jack

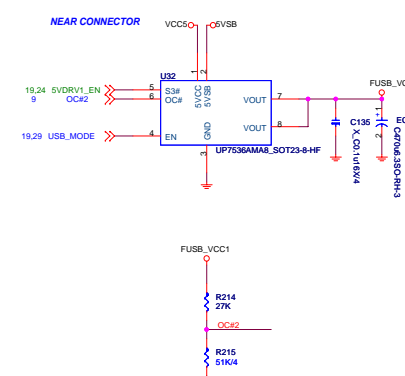
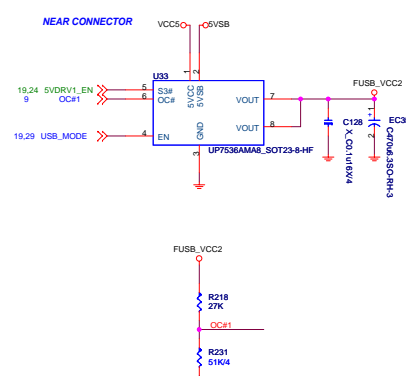
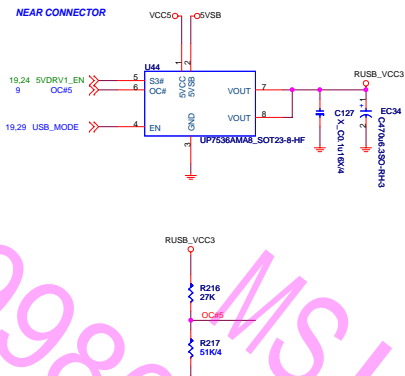
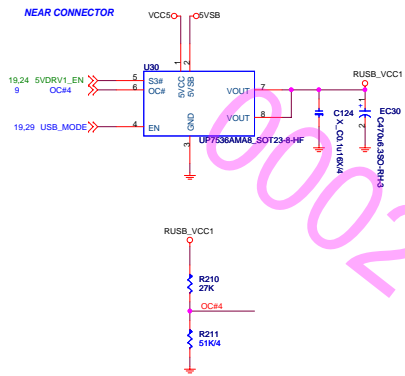


FRONT AUDIO HEADER

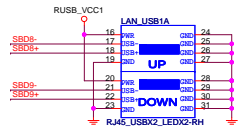


SPDIF OUT OPT+RCA

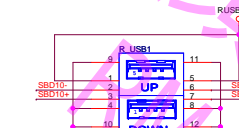




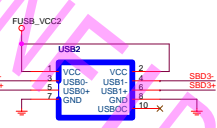
REAR USB PORT 6,7



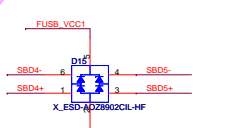
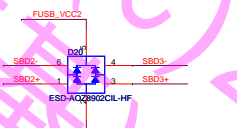
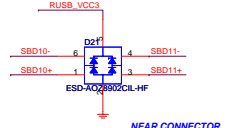
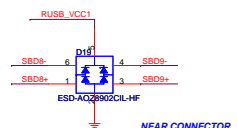
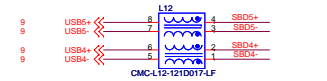
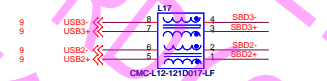
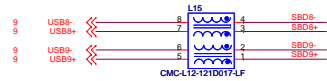
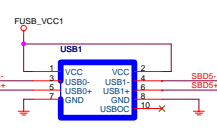
REAR USB PORT 10,11

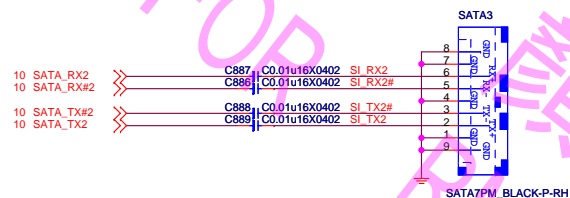
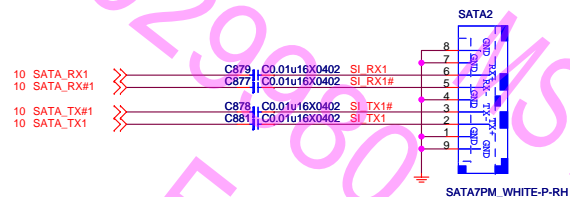
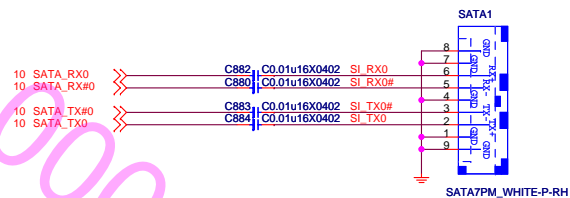


Front USB PORT 2,3

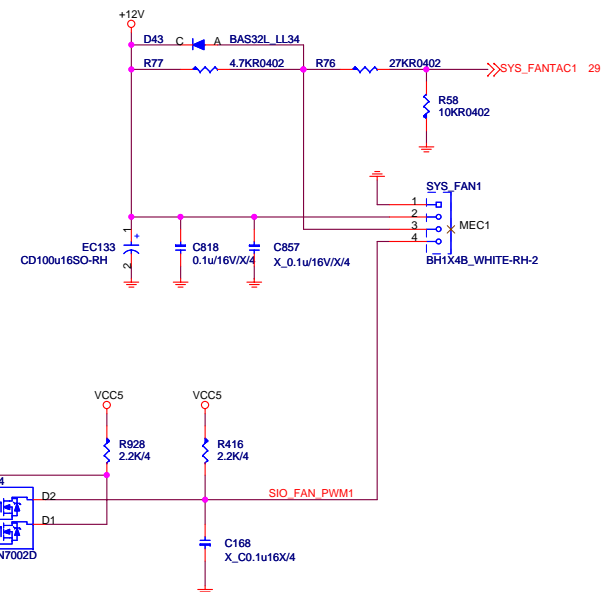


Front USB PORT 4,5

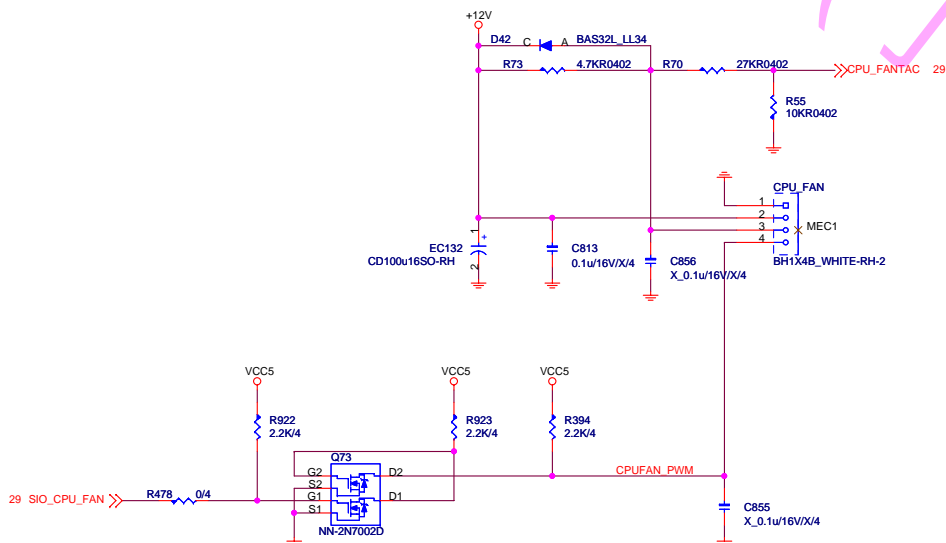




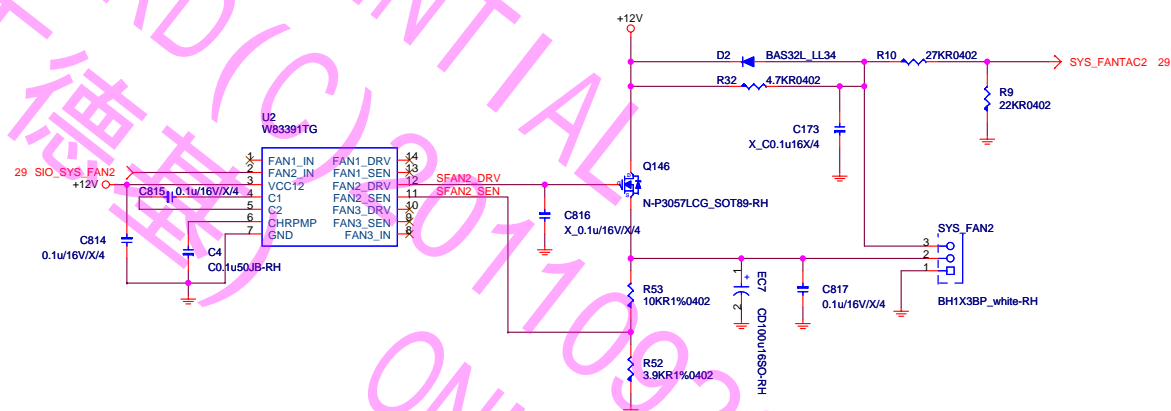
SYS Fan 1



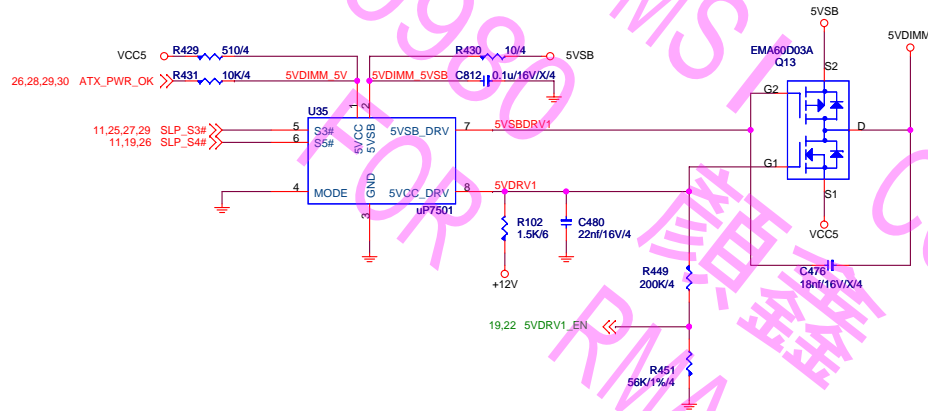
CPU Fan



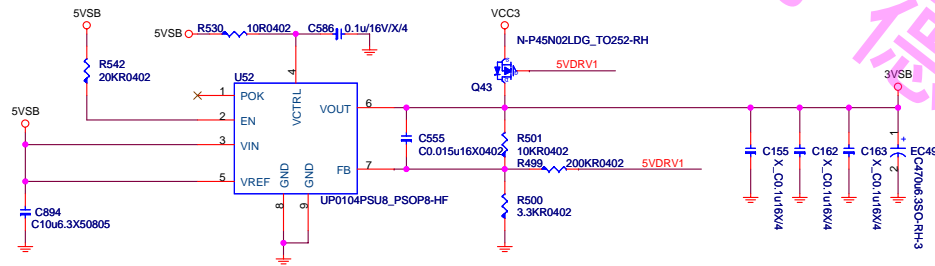
SYS Fan 2



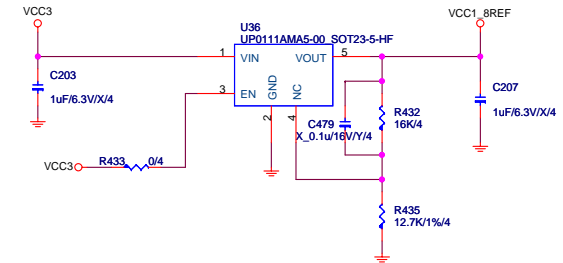
5VDIMM FOR DDR



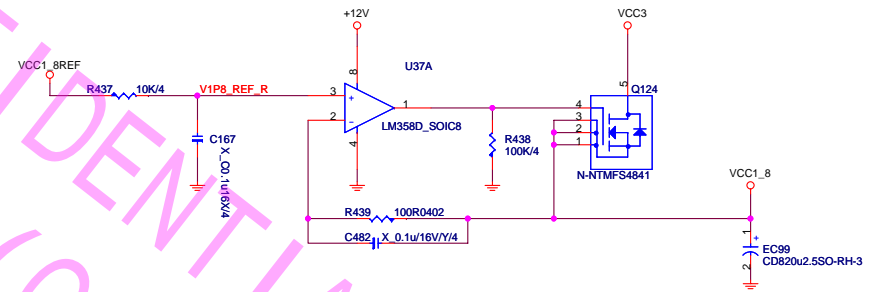
3VSB Power Rail



VCC1_8REF



CPU_PLL_1_8



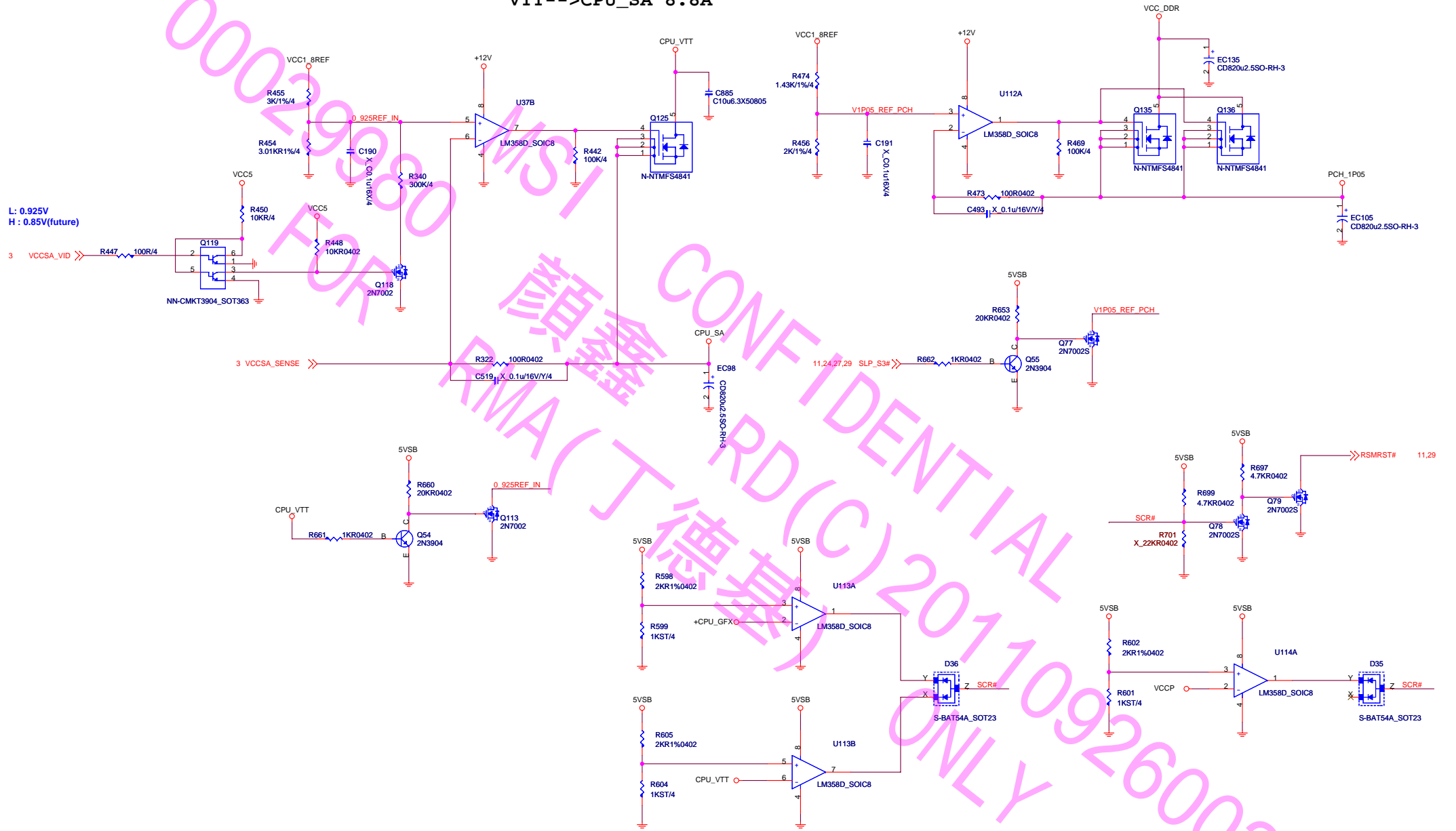
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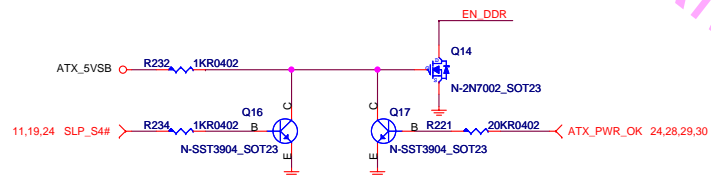
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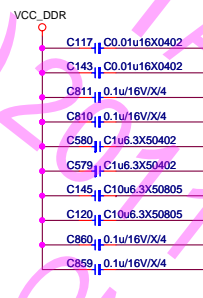
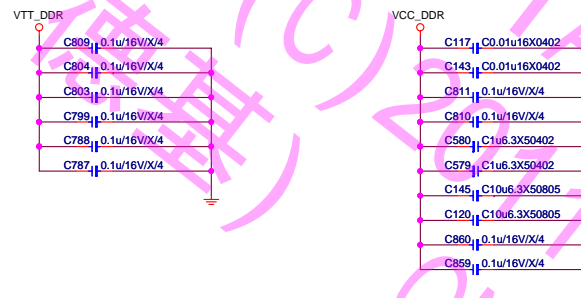
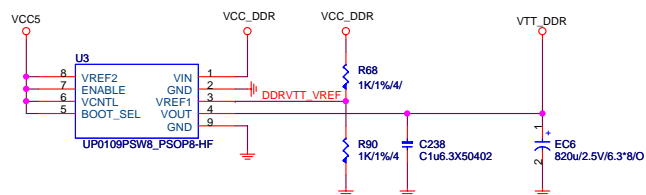
VTT-->CPU_SA 8.8A

DDR-->PCH 6.2A



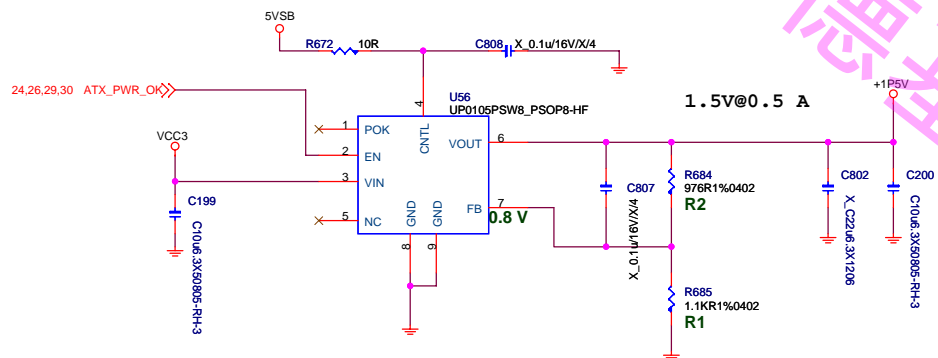
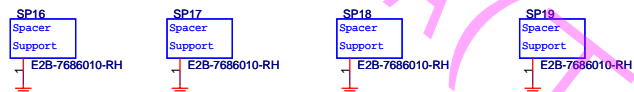
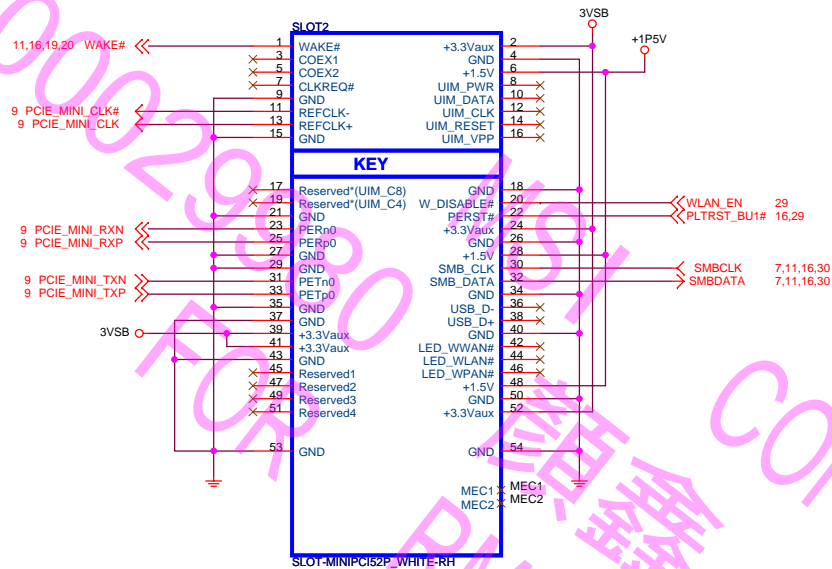


To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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ATX POWER CONNECTOR

ATX POWER CONNECTOR

Diagram showing the ATX Power Connector (PWR1) and its connections to various power rails and signals.

Connections include:

- VCC3
- 12V
- VCC5
- 3VSB
- VCC5
- ATX_5VSB
- +12V
- VCC3
- ATX_PWR_OK (24, 26, 28, 29)
- PWRCONN24P_BLACK-RH-2

Buzzer Circuit

Buzzer Circuit

Diagram showing the Buzzer Circuit (BZ1) and its connections to various components.

Connections include:

- VCC5
- BUZZER-LF
- BAS32L_LL34
- R547 (220R0402)
- R545 (220R0402)
- Q46 (N-MMBT3904_NL_SOT23)
- R544 (2.2KR040)

Front Panel

FRONT PANEL

11 ODD_SW+ ← R213 0/4 1 HDD+ PLED 2 PWR_LED

3 HDD- SLED 4 SUS_LED

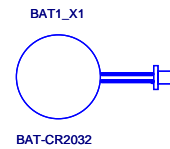
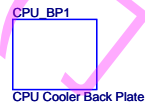
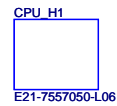
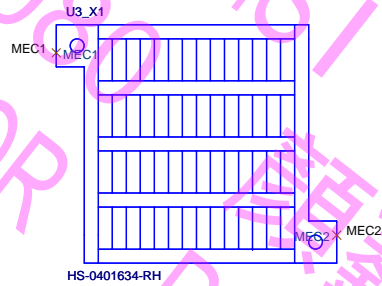
7,11,16,28 SMBCLK 5 RESET- PWSW+ 6 PWRSW+

7,11,16,28 SMBDATA 7 RESET+ PWSW- 8 PWRSW-

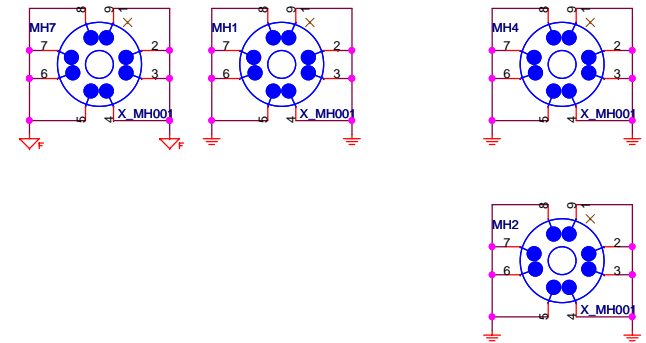
9 NC 9

H2X5[10]M_COLORS-RH

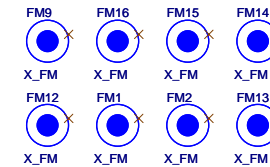
C166 X_C0.1u16X/4



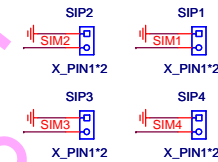
Mounting Holes



Optical Fiducial Marks-120



Simulation




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